REMARKS

Claims 1, 3-14, 16-19, 21-24, and 31-54 remain in this application. Claims 1, 6, 16-19, 21-22, 31, 34, 45, and 48-50 have been amended to more properly define the invention. The amendments are supported by the specification. No new matter has been added. No claims have been cancelled or added. The Applicants respectfully request reconsideration of this application in view of the above amendments and the following remarks.

35 U.S.C. §103(a) Rejection – Gates

The Examiner has rejected claims 1, 4-6 and 9-14, 16-19, 21-24, 31-54 under 35 U.S.C. §103(a) as being obvious over U.S. Patent No. 5,701,409 issued to Gates (hereinafter referred to as "Gates").

Claim 1 and Dependent Claims

Claim 1 recites, "*a plurality of predefined bus stimuli instructions that represent a predefined sequence of bus transactions, wherein each transaction has multiple transaction phases*". Gates does not teach or suggest a **predefined sequence of multiple-phase bus transactions**.

Claim 1 has been amended to make it clear that the bus transactions each have multiple transaction phases. Transaction phases are explained in the patent application as phases such as an arbitration phase, an address phase, a data phase, or the like for a particular bus. Thus, claim 1 is directed to a system to drive a predefined sequence of multiple-phase bus transactions on a bus. The sequence of the commands is significant, since an agent attached to the bus may respond incorrectly to the sequence, as discussed in the application.

Gates does not discuss a predefined sequence of multiple-phase bus transactions. In fact, the use of a sequence of commands is completely foreign to Gates. Gates only discusses the individual commands shown in Figure 7 and is not interested in a predetermined sequence of the commands. Accordingly, the use of a predefined sequence of multiple phase bus transactions is completely foreign to Gates.

Additionally, Gates discusses an entirely different way of making a circuit attached to the bus have an error that has nothing to do with a sequence of commands. The Gates approach entails forcing an error through a bus error generation circuit intentionally inverting a parity bit for each command. The parity bit inversion is done by the incorrect parity control circuits 110 and 209 shown in Figures 3 and 5, respectively. This parity bit is inverted for a single command, rather than a sequence. As one example, the command MTDATAPARERR "Target Write Data Parity Error" forces a targets incorrect parity control circuit to assert an incorrect parity bit. Accordingly, Gates takes an entirely different approach to error generation, based on a single command forcing inversion of a parity bit, which has nothing to do with a predetermined sequence of bus transactions.

Accordingly, claim 1 is believed to be allowable. Claims 3-14 and 32-33 depend from claim 1 and are believed to be allowable therefor as well as for the recitations independently set forth therein.

Claim 16 and Dependent Claims

Claim 16 recites, "*instructions representing a predefined sequence of bus transactions, wherein each transaction has multiple transaction phases*". Accordingly, claim 16 is believed to be allowable for reasons similar to those discussed above for claim 1. Claims 17-19 depend from claim 16 and are believed to be allowable therefor as well as for the recitations independently set forth therein.

Claim 21 and Dependent Claims

Claim 21 recites, "*receiving instruction words representing a predefined sequence of bus transactions, wherein each transaction has multiple transaction phases*". Accordingly, claim 21 is believed to be allowable for reasons similar to those discussed above for claim 1. Claims 22-24 depend from claim 21 and are believed to be allowable therefor as well as for the recitations independently set forth therein.

Claim 31

Claim 31 recites, "*generating a plurality of instruction words corresponding to a predefined sequence of bus transactions, wherein each transaction has multiple phases*". Accordingly, claim 31 is believed to be allowable for reasons similar to those discussed above for claim 1.

Claim 34 and Dependent Claims

Claim 34 recites, "*a representation of a predefined sequence of bus stimuli associated with multiple phase bus transactions*". Accordingly, claim 34 is believed to be allowable for reasons similar to those discussed above for claim 1. Claims 35-47 depend from claim 34 and are believed to be allowable therefor as well as for the recitations independently set forth therein.

Claim 48 and Dependent Claim

Claim 48 recites, "*debug means coupled with the bus for asserting a legal sequence of multiple phase bus transactions on the bus and for allowing determination of an incorrect response to the sequence by the bus agent*". Claim 48 is believed to be allowable because Gates does not discuss a means for allowing determination of an incorrect response to a sequence by a bus agent. Rather Gates discusses forcing an error response to a single instruction with an inverted parity bit. Claim 49 depends from claim 48 and is believed to be allowable therefor as well as for the recitations independently set forth therein.

Claim 50 and Dependent Claims

Claim 50 recites, "*An integrated circuit designed by defining a **legal** sequence of multiple phase bus transactions, asserting signals corresponding to the sequence of bus transactions on a bus, **capturing a response of an integrated circuit to the sequence of bus transactions, analyzing the response to detect a bug associated with an incorrect response to the legal sequence**, and correcting the bug*".

Claim 50 is believed to be allowable for at least the reason that Gates does not teach or suggest **capturing a response to a sequence of multiple phase bus transactions**. Rather, as discussed above Gates discusses forcing an error response by using a single command to invert a parity bit. Claims 51-54 depend from claim 50 and are believed to be allowable therefor as well as for the recitations independently set forth therein.

35 U.S.C. §103(a) Rejection – Gates

The Examiner has rejected claims 3, 7 and 8 under 35 U.S.C. §103(a) as being unpatentable over "Gates". These claims are believed to be allowable for the reasons discussed above.

Conclusion

The Applicants respectfully submit that the rejections have been overcome by the amendment and remark, and that the claims as amended are now in condition for allowance. Accordingly, the Applicants respectfully requests the rejections be withdrawn and the claims as amended be allowed. The Examiner is requested to call Brent E. Vecchia at (303) 740-1980 if there remains any issue with allowance of the case.

Request For An Extension Of Time

The Applicant respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17 for such an extension.

Charge Our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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Date: February 26, 2002

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In The Claims:

The claims have been amended as follows:

1. (Amended) A system comprising:

an instruction memory to store a plurality of predefined bus stimuli instructions[,] [the predefined bus stimuli instructions representing] that represent a predefined sequence [plurality] of bus transactions, wherein each transaction has multiple transaction phases; and

one or more phase generators coupled with a bus and the instruction memory, the one or more phase generators to drive a series of signals on the bus corresponding to the [predefined bus stimuli instructions in a] predefined sequence of bus transactions.

6. (Amended) The system of claim 1, wherein [the at least one of] the one or more phase generators includes at least one digital logic device responsive to the instructions and at least one phase engine to control timing of the bus stimuli.

16. (Amended) A system comprising:

a first means for storing [to store] instructions representing a predefined sequence of bus transactions, wherein each transaction has multiple transaction phases [plurality of predefined bus transactions]; and

second means for driving [to drive] the [plurality of] predefined sequence of bus transactions as signals on the bus.

17. (Amended) The system of claim 16, further comprising third means for storing [to store] data representing predefined responses to signals received from the bus, and wherein the second means implements the predefined responses based on the signals received from the bus.

18. (Amended) The system of claim 16, further comprising fourth means for controlling [to control] the timing of the signals provided to the bus by the second means.

19. (Amended) The system of claim 16, further comprising fifth means for storing [to store] data to be exchanged with agents on the bus, wherein the second means transmits data from the fifth means in response to the instructions stored in the first means.

21. (Amended) A method [for testing a bus] comprising:

receiving instruction words [corresponding to predefined bus stimuli, the predefined bus stimuli] representing a [plurality] predefined sequence of bus transactions, wherein each transaction has multiple transaction phases; and

executing the predefined sequence [plurality] of bus transactions by converting the instruction words to signals and driving the signals on the bus.

22. (Amended) The method of claim 21, further comprising:

defining a sequence of [desired] bus transactions; and

assembling the sequence of [desired] bus transactions into instruction words wherein the sequence of bus transactions are executed when the instruction words are converted to signals and driven on the bus.

31. (Amended) A method comprising:

generating a plurality of instruction words corresponding to a predefined sequence of bus transactions, wherein each transaction has multiple phases;

storing the instruction words in a memory; and

executing the predefined sequence of bus transactions by converting the plurality of instruction words into signals and driving the signals onto the bus in the predefined sequence.

34. (Amended) A system comprising:

an interface to a host computer to receive a representation of a predefined sequence of bus stimuli associated with multiple phase bus transactions;

a memory to store the representation;

logic to translate the representation into the sequence of bus stimuli; and

a phase generator to provide the predefined sequence of bus stimuli to the bus.

45. (Amended) The system of claim 34, wherein the predefined sequence of bus stimuli are correspond to three bus transactions [comprises a plurality of bus transactions that each comprise a plurality of transaction phases].

48. (Amended) A system comprising:

a bus to receive bus transactions;

a bus agent coupled with the bus; and

debug means coupled with the bus for asserting [to assert] a legal sequence of multiple phase bus transactions on the bus and [to detect] for allowing determination of an incorrect response to the sequence [from] by the bus agent.

49. (Amended) A bus agent [redesigned] designed to eliminate a bug [detected] determined by the system of claim 48.

50. (Amended) An integrated circuit designed by defining a legal sequence of multiple phase bus transactions, asserting signals corresponding to the sequence of bus transactions on a bus, capturing a response of [the] an integrated circuit to the sequence of bus transactions, analyzing the response to detect a bug associated with an incorrect response to the legal sequence, and correcting the bug.